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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,789	03/17/2004	Cengiz A. Palanduz	42.P17181X	8049

8791 7590 10/19/2005

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EXAMINER	
HA, NGUYEN T	

ART UNIT	PAPER NUMBER
2831	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,789	PALANDUZ ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-9 are rejected under 35 U.S.C. 102(a) as being unpatentable over Chakravorty (US 6,611,419) in view of Farooq et al. (US 6,791,133).

Regarding claim 1, Chakravorty discloses a substrate of an integrated circuit package (figure 3), comprising:

- a base structure/substrate (310) having upper and lower sides (326 & 329) and a plurality of via opening (315 & 327) formed therein;
- a conductive via in each via opening, the conductive vias (315 & 327) including at least power and ground vias (column 5, lines 20-33) (figure 3); and
- first and second capacitor (330) structures on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes (329 and 326, column 5, lines 24-33) and a dielectric layer (340) between the power and ground planes, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively (figure 3).

Chakravorty lacks the base structure including at least a portion having a low k-value and the dielectric having a high k-value.

Farooq et al. teach a base/substrate (304) including at least a portion having a low k-value and a dielectric having a high k-value (column 6, lines 12-13 and column 5, lines 8-9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the assembly as taught by Farooq et al. in Chakravorty in order to use under high temperature, and increase the conductivity for the capacitor.

Regarding claim 2, Chakravorty discloses the base structure is made of a sintered ceramic material (column 7, lines 9-13).

Regarding claim 3, Chakravorty discloses the vias includes signal vias, each signal via being electrically disconnected from both the power and ground planes (figure 3).

Regarding claim 4, the teaching of Chakravorty in view of Farooq includes all the claimed limitations discussed above in claim 3, and further disclose the signal vias being formed in the portion have the low k-value material (figure 3).

Regarding claim 5, Chakravorty discloses an integrated circuit package (figure 3) comprising:

- a base structure/substrate (310) having upper and lower sides (326 & 329) and a plurality of via opening (315 $ 327) formed therein;
- a conductive via in each via opening (figure 3), the conductive vias (315 & 327) including at least power and ground vias (column 5, lines 20-33); and
- first and second capacitor structures (330) on the upper and lower sides of the base structure respectively, each capacitor structure including conductive power and ground planes (326 & 329, column 5, lines 24-33) and a dielectric layer (340) between the power and ground plane, the power and ground planes being electrically connected to at least one of the power and ground vias, respectively; and a dielectric having an integrated circuit formed therein mounted on the substrate (figure 3).

Chakravorty lacks the base structure including at least a portion having a low k-value and the dielectric having a high k-value.

Farooq et al. teach a base/substrate (304) including at least a portion having a low k-value and a dielectric having a high k-value (column 6, lines 12-13 and column 5, lines 8-9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the assembly as taught by Farooq et al. in Chakravorty in order to use under high temperature, and increase the conductivity for the capacitor.

Regarding claim 6, Chakravorty discloses the substrate (310) is an interposer substrate, further comprising: a package substrate, the interposer substrate being mounted to the package substrate (figure 3).

Regarding claim 7, Chakravorty discloses the vias are connected to contacts on the package substrate without and x-y transformation (figure 3).

Regarding claim 8, Chakravorty discloses the vias includes signal vias, each signal via being electrically disconnected from both the power and ground planes (figure 3).

Regarding claim 9, the teaching of Chakravorty in view of Farooq includes all the claimed limitations discussed above in claim 8, and further disclose the signal vias being formed in the portion have the low k-value material (figure 3).

Citation Relevant of Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

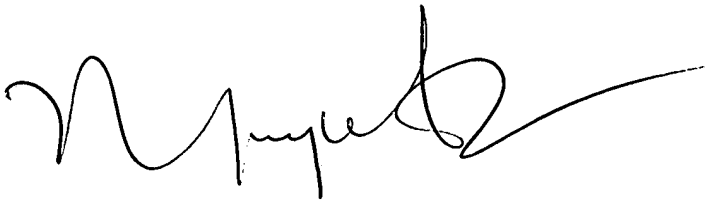
a. Hale et al. (US 6,407,929) disclose an electronic package having embedded capacitors and method of fabrication therefor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nguyen T. Ha
October 17, 2005